Abstract: Power consumption and Area reduction play a major role in sequential circuit design. A novel design and analysis of a shift register using pulsed latches with reduced power and area is proposed. To reduce the area the traditional data flip-flops are substituted with pulsed latches. The use of various non-overlap delay pulsed clock signals substituted by the traditional single pulsed clock signals by this design solves the timing issues in pulsed latches. In the standard system, shift register uses a single pulsed clock signal for data transition, which consumes additional power. The shift register uses a small number of the pulsed clock signals and combines the latches to many sub shifter registers and exploitation further temporary storage latches. To minimize power consumption various non-overlaps delayed pulsed clock signal design is proposed for data synchronization in an exceedingly multi-bit shift register. The proposed system is designed by using HSpice tool.

Keywords: Flip-Flop; Pulsed Clock; Pulsed Latch; Shift Register

I. INTRODUCTION

In digital design flip-flops and latches are basic storage elements. Flip flops are precarious timing elements in digital circuits which have a great impact on speed and power consumption. In VLSI chip design reducing power has become an important consideration of a performance and area. The Shift register is a type of sequential circuit it is mainly used for storage or transfer digital data.

An M-bit shift register consists of M-data flip-flops which are connected in series. The Implementation of the M-data flip-flop is a less important element to regulate the capability of the total synchronous circuit than the area and power consumption, as a result, there is no circuit present between flip-flops within the register. To reduce the area and power consumption, the smaller flip-flop is used for the register. In this flip-flops the transistor are more compared to pulsed latches so that the circuit has more switching and power consumption is high.

Flip-flops are replaced by pulsed latch in several applications because pulsed latches are smaller than flip flops. The use of multiple non-overlap delays pulsed clock signals substituted by the traditional single pulsed clock signals by this design solves the timing problem in pulsed latches. The shift register uses a less number of the pulsed clock signals and combines the latches to many subshift registers and exploitation further temporary storage latches.

Fig. 1. (a) Master–slave flip-flop. (b) Pulsed latch.

The rest of the paper describes the proposed shift register architecture in section II. Results are presented in section III. The conclusion is given in section IV.

II. PROPOSED SHIFT REGISTER

A master–slave flip-flop using two latches in Fig. 1(a) can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal in Fig. 1(b). All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master–slave flip-flop. The pulsed latch is an attractive solution for a small area and low power consumption. The pulsed latch cannot be used in shift registers due to the timing problem, as shown in Fig. 2. The shift registers in Fig. 2(a) consists of several latches and a pulsed clock signal (CLK_pulse). The operation waveforms in Fig. 2(b) show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the input signals of the first latch (IN) is constant during the clock pulse width (Tpulse). But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width.
Fig. 2. The shift registers with latches and a pulsed clock signal. (a) Schematic. (b) Waveforms.

One solution for the timing problem is to add delay circuits between latches, as shown in Fig. 3(a). The output signal of the latch is delayed and reaches the next latch after the lock pulse. As shown in Fig. 3(b) the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width, but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant input signals during the clock pulse and no timing problem occurs between the latches. However, the delay circuits cause large area and power overheads.

Fig. 4. Shift register with latches and delayed pulsed clock signals. (a) Schematic. (b) Waveforms.

The proposed shift register is divided into M subshift registers for reducing the number of delayed pulsed clock signals. The schematic for proposed shift register is shown in Fig. 5(a) and its operating waveform is shown in Fig. 5(b). A 4-bit sub shifter register consists of five latches and it performs shift operations with five non-overlap delayed pulsed clock signals. In the 4-bit sub-shift register #1, four latches store 4-bit data and the last latch stores 1-bit temporary data which will be stored in the first latch of the 4-bit sub-shift register. The proposed shift register reduces the number of delayed pulsed clock signals significant.

The maximum clock frequency in the conventional shift register is limited to only the delay of flip-flops because there is no delay between flip-flops. Therefore, the area and power consumption are more important than the speed for selecting the flip-flop. The proposed shift register uses latches instead of flip-flops to reduce the area and power consumption.

The pulse generation circuit used in the proposed shift register has a serially connected chain of delay elements, the first delay element for receiving an input pulse. It has a plurality of logic gates with each logic gate having one input coupled to the output of one delay element in the chain. The other input is coupled to the output of the next delay element in the chain. When the input pulse is received, the outputs of the logic gates form a plurality of non-overlapping pulses.
A pulse generator circuit includes a delay circuit responsive to an input signal for producing an output signal after a predetermined delay time, a first logic circuit responsive to the input signal and this output signal for producing an output signal having a first logic state when both of the input signal and the output signal from the delay circuit are of the first logic value, a second logic circuit responsive to the input signal and the output signal from the delay circuit are of the first logic state when both the input signal and the output signal from the delay circuit are of the first logic value, and a third logic circuit responsive to the output signal from the first logic circuit and to the output signal from the second logic circuit for producing an output signal having a first logic state when both of the output signal from the first logic circuit and the output signal from the second logic circuit are concurrent of the second logic value.

The circuit for the pulse generation circuit and its timing diagram is shown in the Fig.6 and Fig.7.

**Fig. 5. Proposed shift register. (a) Schematic. (b) Waveforms.**

**Fig. 6. Delayed pulsed clock generator.**

**Fig. 7. Minimum clock cycle time of the proposed shift register.**

### III. CONCLUSION

The design and analysis of a shift register using pulsed latches with reduced power and area are proposed. In order to reduce the area, the traditional data flip-flops are substituted placed with pulsed latches. The use of various non-overlap delay pulsed clock signals substituted by the traditional single pulsed clock signals by this design solves the timing problem in pulsed latches. In the standard system, shift register uses a single pulsed clock signal for data transition, which consumes additional power. The shift register uses a small number of the pulsed clock signals and combines the latches to many sub shifter registers and exploitation further temporary storage latches. To minimize power consumption multiple non-overlap delayed pulsed clock signal design is proposed for data synchronization in an exceedingly multi-bit shift register.

### IV. REFERENCES


