Investigating of Multi Level Topology with Reduced Number of Switches

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Abstract:
A novel three stage multilevel inverter with a little number of exchanging gadgets is proposed. Extensive electrical drives and utility application require propelled power gadgets converter to meet the powerful requests. Subsequently, multilevel force converter structure has been presented as an option in high power and medium voltage circumstances. A multilevel converter accomplishes high power rating as well as enhances the execution of the entire framework as far as sounds. In this paper the proposed inverter can yield more quantities of voltage levels with diminished number of changes when contrasted with course H-span inverter, which brings about decrease of establishment cost and have effortlessness of control framework. At long last, the reenactment and trial results approve the idea of this new topology.

Keywords:
PWM, SPWM, Cascade H-Bridge(CHB), Matlab Simulation, Multilevel Inverter.

INTRODUCTION
The diverse sorts fall multilevel inverter topology are accessible. A nonstop advancement of multilevel converter to drive high voltage and high current mechanical applications[1]. These days, multilevel inverter are great answers for force applications because of the way that they can accomplish high power utilizing propelled power semiconductor[1]. Be that as it may, the principle disservice of the multilevel inverter more number of voltage level lead to expand the fundamental switches, many-sided quality of control strategy and DC join capacitor voltage lopsidedness .There are a few focal points contrasted and customary or routine force change techniques. In multilevel inverter the separated DC sources or bank of arrangement capacitors are utilized. Disengaged DC sources are accessible from the Photovoltaic cell or corrected yield from the three stage primary supply. The Photovoltaic force transformation is one of the best suitable applications for fall H Bridge multilevel inverter. The littler voltage level increment to lead the yield quality regarding decrease the voltage stress (dv/dt), Electromagnetic Interference (EMI) and draw information current with low bending. However these focal points are extremely alluring to the modern application and analysts everywhere throughout the world adding to enhance the execution (control rearrangements, decreased THD, less number of parts and swell current) of multilevel inverter[1]. Since a decade ago the enthusiasm of the specialists are adding to further advancement of another multilevel converters topology with remarkable balance methodologies. The specialists from all over world presenting number of later and progressed multilevel inverters topologies. There are a few multilevel converters are marketed for high power applications, for example, Flexible AC transmission systems(FACTS) Controllers, Train Traction, Automotive applications, renewable vitality power transformation and transmission [2]-[4] and so on. Some new multilevel inverter topologies are recommended with various working strategies with diminished switches[5]-[6]. In spite of the fact that the topology required distinctive voltage rating switches contrasted and traditional CHB topology. It likewise required the objective determination.
manufacturing the Multi winding transformer is high[5]. The topology includes with H-Bridge and Auxiliary bidirectional switch, to reduce the power circuit complexity and modulator circuit development[8]. Even though the number of switches are more compare with the proposed topology.

THE PROPOSED MULTILEVEL INVERTER

As the most critical part in multilevel inverters are switches which characterize the dependability, circuit size, cost, establishment territory and control multifaceted nature. The quantity of required switches against required voltage levels is imperative component in the configuration. To give countless levels without expanding the quantity of extensions, another force circuit topology and a suitable technique to decide the dc voltage sources level for symmetrical and lopsided multilevel converter are proposed in this paper. The proposed circuit likewise gives diminished voltage weight on the switch by the arrangement setup of the connected bidirectional switches. This consequently upgrades the safety from overvoltage and dv/dt breakdown. Fig. 2 demonstrates a setup of the proposed symmetrical multilevel inverter. If there should arise an occurrence of Fig. 3, it creates 11-level formed yield voltage wave.

For expanding yield voltage levels one power supply might be included with one switches as it were. This proposed strategy is unique in relation to the technique , since it has less number of bidirectional switch and not quite the same as the ordinary inverters and strategy in [2], since it has less number of switches.

The effective number of output voltage steps (Nstep) in symmetric multilevel inverter is:

\[ N_{\text{step}} = 2n - 1 \]

Where n represented the number of dc supplies and the maximum output voltage (V_{omax}) of this n cascaded multilevel inverter is:

\[ V_{omax} = (n - 1)V_{dc} \]

Vo can be increased by connecting the N basic circuit given in Fig 2 in series as shown in Fig. 4. In this case only two switch of each unit turns on for the operation of the converter at any given time.

By. 5, this topology is unique in relation to the ordinary inverters and the strategy in [2] since it has less of switches. While the proposed topology is intended to deliver the aggregate dc by interfacing the regulation dc sources (V_{dc1}) to one and only of remaining supplies (V_{dc2} ... V_{dcK}), the configuration introduced in [3] depends on setting up an arrangement association of any number of the supplies V_{dc1} to V_{dcK}. The new plan applies less number of bidirectional changes which prompts lessened misfortunes and conquers the uneven voltage step issue.

The new basic element (one stage) of asymmetric multilevel inverter with Kdc sources (cells).

\[ V_{dc1} = V_{dc} \]
\[ V_{eq} = 2(j - 1)V_{dc} \quad \text{if } j = 2,3, ... K \]
As opposed to strategy [23] by utilizing this mathematical statement all levels can be gotten without losing any level which decreases THD at the yield. The quantity of yield voltage levels in a fell multi-level inverter is then:

\[ N_{\text{Step}} = \frac{2V_{\text{dc}}}{V_{\text{dc}}} + 3 \]  

(11)

The maximum output voltage \( V_{\text{o,max}} \) of this new topology is:

\[ V_{\text{o,max}} = (V_{\text{dc}} + V_{\text{dc}}) \]

By adding The number of the basic element is shown in Fig. 5 is connected in series same as shown in Fig. 4, to increase the output voltage. The resulting proposed asymmetrical inverter configuration can generate a stepped voltage waveform without any loss at any level.

**MODULATION TECHNIQUE:**

The proposed system can be run with existing modulation technique Alternative Phase Opposition Disposition (APOD). If \( M=7 \) (M is number of Level) the required carrier waveforms is \( M-1=6 \).

**Figure 2(d) APOD Modulation**

There are several unique carrier based PWM (CBPWM) techniques are available for multilevel inverter. One of the most common methods is APOD (Alternative Phase Opposition Disposition). APOD carriers in adjacent side are phase shifted by \( 180^\circ \) and CBBPWM required S-1 triangular carrier waveform and S is the number of voltage level as shown in Figure 2(d).

**CASCADED H-BRIDGE MULTILEVEL INVERTER STRUCTURE**

Traditional fell multilevel inverters is a standout amongst the most essential topologies in the group of multilevel and multi-beat inverters [1]. The course topology permits the utilization of a few levels of DC voltages to combine a fancied AC voltages. The DC levels are thought to be indistinguishable since every one of them are either an energy units or photovoltaics, normal decision, batteries, and so forth [2]. A fell multi-level inverter comprises of various Hbridge inverter units with independent dc hotspot for every unit and it is associated in course or arrangement as appeared in Fig. 1 [2]. The full-connect (H-span) topology appeared in Fig. 1 is utilized to orchestrate a three one of a kind yield voltages \( (+V_{\text{dc}}, -V_{\text{dc}} \text{ and zero}) \), by associating the dc source to air conditioning yield side by various mixes of the four switches S1, S2, S3, and S4. The general yield voltage of multilevel inverter is given by:

\[ V_{\text{o}} = V_{\text{o}1} + V_{\text{o}2} + V_{\text{o}3} + V_{\text{o}n} \]

**Fig. 6. Configuration of cascaded multilevel inverter**

On the off chance that all dc voltage sources in Fig. 6 equivalent to \( V_{\text{dc}} \), the inverter is known as symmetric multilevel inverter and The quantity of yield stage voltage levels \( N_{\text{Step}} \) in a course inverter is characterized by:

\[ N_{\text{Step}} = 2n + 1 \]

Where \( n \) is the number of separate dc sources (photovoltaic modules or fuel cells) or the number of full-bridges and the maximum output voltage \( (V_{\text{o,max}}) \) of this \( n \) cascaded multilevel inverter is:

\[ V_{\text{o,max}} = nV_{\text{dc}} \]

For deviated fell multilevel inverter, DC voltage wellsprings of various cells are non-measure up to. Unbalanced inverter gives an expanded number of voltage levels for the same cells number than its symmetric partner. On the off chance that the DC voltages of individual cells Fig. 1 are chosen by geometric movement with a component of a few .For \( n \) fell multilevel inverters, then the quantity of voltage steps check is:

\[ N_{\text{Step}} = 2^{n+1} - 1 \text{ if } V_j = 2^{j-1}V_{\text{dc}} \text{ for } j = 1, 2, ..., n \]  

(4)

\[ N_{\text{Step}} = 3^{n+1} - 1 \text{ if } V_j = 3^{j-1}V_{\text{dc}} \text{ for } j = 1, 2, ..., n \]  

(5)

The maximum output voltages of these \( n \) cascaded multilevel inverters are:

\[ V_{\text{o,max}} = (2^n - 1)V_{\text{dc}} \text{ if } V_j = 2^{j-1}V_{\text{dc}} \text{ for } j = 1, 2, ..., n \]  

(6)

\[ V_{\text{o,max}} = (3^{n-1})V_{\text{dc}} \text{ if } V_j = 3^{j-1}V_{\text{dc}} \text{ for } j = 1, 2, ..., n \]  

(7)
Comparing the Eqs. (2)–(7), it can be seen that the asymmetric multilevel inverters can generate more voltage steps and higher maximum output voltage with the same number of bridges.

**BASIC CIRCUIT DIAGRAM**

![BASIC CIRCUIT DIAGRAM](image1)

**CONCLUSION**

A novel three stage multilevel inverter topology has been proposed in this paper. The most vital component of the framework is being helpful for extending and expanding the quantity of yield levels just with less number of switches. This technique results in the diminishment of the quantity of switches, misfortunes, cost furthermore put. With present exchanging calculation, the multilevel inverter creates almost sinusoidal yield voltage with low consonant substance.

**REFERENCE**


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