To Solve the Timing Problem Between Pulsed Handlers

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Abstract: This paper solves the timing problem between pulsed latches through the utilization of multiple non-overlap postponed pulsed clock signals instead of the traditional single pulsed clock signal. The shift register uses a small amount of the pulsed clock signals by grouping the latches to many sub shifter registers and taking advantage of additional temporary storage latches. The timing problem can be reduced by replacing flip-flops with pulsed latches. A 4-bit shift register was design using pulsed latches with help of dsc tool.

Keywords: Flip-Flop; Pulsed Clock; Pulsed Latch; Shift Register.

I. INTRODUCTION

A shift register may be the fundamental foundation inside a VLSI circuit. Shift registers are generally utilized in many programs, for example digital filters, communication receivers, and image processing ICs. Lately, as how big the image data is constantly on the increase because of the popular for high quality image data, the term entire shift register increases to process large image data in image processing ICs. A picture-extraction and vector generation VLSI nick use a 4K-bit shift register. A Ten-bit 208 funnel output LCD column driver IC utilizes a 2K-bit shift register. A 16-megapixel CMOS image sensor utilizes a 45K-bit shift register. As the word entire shift register increases, the region and power use of the shift register become important. The architecture of the shift register is very simple. An N-bit shift register consists of series connected N data switch-flops. The rate from the switch-flop is less important compared to area and power consumption because there’s no circuit between switch-flips in the shift register. The switch-flop is appropriate for that shift register to lessen the region and power consumption. Lately, pulsed latches have changed switch-flips in lots of programs, because a pulsed latch is a lot smaller sized than the usual switch flop. However the pulsed latch can’t be utilized in a shift register because of the timing problem between pulsed latches. This paper solves the timing problem using multiple non-overlap postponed pulsed clock signals instead from the conventional single pulsed clock signal. The shift register uses a small amount of the pulsed clock signals by grouping the latches to many sub shifter registers. Registers and using additional temporary storage latches.

Figure 1.1: Schematic diagrams of (a) Master-slave flip flop. (b) Pulsed latch

II. PROPOSED SHIFT REGISTER

A master-slave flip-flop using two latches in fig.1 (a) can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal in fig.1 (b). However the second latch comes with an uncertain output signal (Q2) because its input signal (Q1) changes throughout the clock pulse width. One solution for that timing issue is to include delay circuits between latches. The output signal of the latch is postponed and reaches the following latch after the clock pulse. The output signals from the first and second latches (Q1 and Q2) change throughout the clock pulse width, however the input signals from the second and third latches (D2 and D3) become identical to the output signals of the third and fourth latches (Q1 and Q2) following. As a result, all latches have constant input signals.
throughout the clock pulse with no timing problem happens between your latches.

Another solution is by using multiple non-overlaps delayed pulsed clock signals. The postponed pulsed clock signals are produced whenever a pulsed clock signal goes through delay circuits. Each latch utilizes a pulsed clock signal which is postponed in the pulsed clock signal utilized in its next latch. Therefore, each latch updates the information after its next latch updates the information. Consequently, each latch includes a constant input during its clock pulse with no timing problem happens between latches. However, this solution also requires many delay circuits inside a lengthy shift register, at the end from the wire, the time pulse shape is degraded because their rising and falling occasions from the clock pulse increase because of the wire delay.
the operation waveforms in the proposed shift register. Five non-overlap delayed pulsed clock signals are clock signals.

![Fig 2.3 Proposed shift register](image1)

![Fig 2.4: 4-Bit implementation in DCSH Tool](image2)

![Fig 2.5: Output waveform](image3)

### III. CONCLUSIONS

This paper solves the timing problem between pulsed latches through the utilization of multiple non-overlap postponed pulsed clock signals instead of the traditional single pulsed clock signal. The shift register uses a small amount of the pulsed clock signals by grouping the latches to many sub shifter registers and taking advantage of additional temporary storage latches. The timing problem can be reduced by replacing flip-flops with pulsed latches. A 4-bit shift register was design using pulsed latches in dsch tool successfully and output waveforms are graphically shown in above.

### IV. REFERENCES


