Low-Power Programmable PRPG with Test Compression Capabilities

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Abstract: This paper describes a new programmable low power test compression method that allows shaping the test power envelope in a fully predictable, accurate, and flexible fashion by adapting the existing logic BIST infrastructure. The proposed hybrid scheme efficiently combines test compression with logic BIST, where both techniques can work synergistically to deliver high quality test. Experimental results obtained for industrial designs illustrate feasibility of the proposed test scheme and are reported herein.

Keywords: Built-In Self-Test; Hybrid Low Power Compression; Low Power Test; Test Data Compression; Scan-Based Test; Toggling;

I. INTRODUCTION

Testing assumes to be a basic part within the field of production. The event of defect in VLSI circuit outcome in testing each chip. The defects that may occur in VLSI chips may cause design errors, material defect, malfunctioning of equipment. As the size of VLSI chips is compressing day by day the demand on power and area utilization is more hence testing is mandatory. Testing can be performing internally or externally. Outdoor testing be able to perform by utilizing Automatic Test Equipment (ATE). The test vectors are produced utilizing ATE in addition to be connected to Circuit under Test (CUT). Then the result is analyze by CAD Tool. The disadvantage of performing test utilizing ATE is longer era required for test and high cost of hardware. Consequently here is a movement from outdoor testing to the indoor testing. Indoor testing can be performing by Built in Self-Test (BIST). While testing BIST reduce difficulties and complication that occurred during circuit testing. BIST can partition the device into umber of levels and performs testing

In digital systems power and energy utilization is superior in test form than in system form. At some phase in self-test power utilization is more by a load since many switching node activity is caused by the random patterns. While during power saving mode a little modules are activated at the meantime. Power supply and casing of a circuit are cost concentrated par t which has to be measured with peak power utilization and dissipation throughout BIST process.

BIST might be reuse throughout the system era, intended for remote application. The life time of the BIST depends on life time of batteries.

Fig.1 Architecture of BIST

The generic block diagram of a BIST is shown in Fig. 1.BIST solution consists of several blocks given below

Circuit under Test (CUT): It is the part of the circuit tested in BIST mode. It can be combinational, sequential or a memory. During testing process on CUT an actual circuit signature is generated and then compare through the high-quality machine signature to decide whether CUT is defective.

Test pattern generator (TPG): This is a one of the basic block of BIST circuit to be tested in which data analysing and compressing has been done. The fault that was generated from various fault that occurred is a direct function of test patterns resulted by the test pattern generator (TPG) and applied to the CUT. Here a Linear Feedback shift register usually generate patterns this patterns are generated in pseudo random fashion.

Test Controller: It is the one of the main block in BIST system which controls the overall system for test execution. It provides signal to control all blocks. If control signal is 0 then BIST enters into test mode. If control signal is 1 then BIST enters into normal mode

Response Analyzer: It acts as a comparator with stored responses. Compares the stored response with the tested output and shows whether the chip passes or fails the test.
This paper presents a fully programmable low power test compression scheme that is integrated in every way with a power-aware pseudorandom test pattern generator developed for BIST applications. As a result, not only its hardware penalty is virtually none, but it also creates an environment that can be used to arrive at an efficient hybrid solution combining advantages of scan compression and logic BIST.

II. BASIC ARCHITECTURE OF PRPG

Fig. 2 shows a block diagram of a low power PRPG structure. An n-bit ring generator (or alternatively a linear feedback shift register) and a phase shifter feeding scan chains form a kernel of the circuitry producing the pseudorandom test patterns. Furthermore, n hold latches are placed between the ring generator and the phase shifter. Each hold latch is individually controlled through a corresponding stage of an n-bit toggle control register. A given latch is transparent for data going from the ring generator to the phase shifter as long as its enable input is asserted. It is said to be in the toggle mode. When the latch is disabled, it captures and saves, for a number of clock cycles, a corresponding bit of the generator, thus driving the phase shifter (and possibly some scan chains) with a constant value. It is now in the hold mode. Clearly, a given scan chain remains in a low-power mode provided disabled latches exclusively drive the corresponding XOR gate forming a phase shifter output. The fraction of hold latches in the toggle mode determines finally a scan switching activity.

![Fig 2: Low power PRPG Architecture](image)

The control register is reloaded once per pattern with the content of an additional shift register. The enable signals injected into the shift register are produced in a probabilistic fashion by using the ring generator and a programmable set of weights (implemented by means of weighted logic V in Fig. 1). A 4-bit register Switching is employed to activate weighted logic, and allows selecting a user-defined level of switching activity. Simple logic associated with the same register detects a code used to switch the low power functionality off. Given only 15 switching codes, the resultant 15 different toggling rates may not always be acceptable. Therefore, a shifting period of every test pattern is a sequence of alternating hold and toggle intervals. A basic T-type flip-flop moves the generator back and forth between these two states as shown in Fig. 2.If it is set to 0, the generator enters the hold period with all latches disabled (through AND gates) regardless of the control register content. If the T flip-flop is set to 1 (the toggle period), then the latches enabled through the shift register can pass test data moving from the ring generator to the scan chains. Two additional parameters kept in 4-bit Hold and Toggle registers determine how long the generator remains either in the hold mode or in the toggle mode, respectively. To terminate either mode, a 1 must occur on the T flip-flop input. This pseudorandom signal is produced by weighted logic H driven by the Toggle and Hold registers. The T flip-flop allows selecting one of these registers as a source of control data to possibly change the operational mode of the generator in the next cycle. For example, when in the toggle mode, we observe the Toggle register. Once weighted logic H outputs 1, the flip-flop toggles, and all hold latches freeze in the last recorded state. They will remain in this state until another 1 occurs on the weighted logic output. The random occurrence of this event is now related to the content of the Hold register indicating when to terminate the hold mode.

III. LP-DECOMPRESSOR

In order to facilitate test data decompression while preserving its original functionality, the circuitry of Fig. 2 has been re-architected. This is illustrated in Fig. 3. The core principle of the new decompressor is to disable both weighted logic blocks (V and H) and to deploy deterministic control data instead. In particular, the content of the toggle control register can now be selected in a deterministic manner due to a multiplexer placed in front of the input of the shift register. Furthermore, the Toggle and Hold registers are employed to alternately preset a 4-bit binary down counter, and thus to determine durations of the hold and toggle phases. When this circuit reaches the value of zero, it causes a dedicated signal to go high in order to toggle the T flip-flop. The same signal allows the counter to have the input data kept in the Toggle or Hold register entered as the next state.

Both, the down counter and the T flip-flop need to be initialized every test pattern. The initial value of the T flip-flop decides whether the decompressor will begin operate either in the toggle or in the hold mode, while the initial value of the counter, further referred to as an offset, and determines that mode’s duration. As can be observed, functionality of the T flip-flops remains the same as that of the low
power PRPG (see Section 2) but two cases. First of all, the encoding procedure (see Section 4) may completely disable the hold phase (when all hold latches are blocked) by loading the Hold register with an appropriate code, for example, 0000. If detected (No Hold in the figure), it overrides the output of the T flip-flop by using an additional OR gate, as shown in Fig. 3. As a result, the entire test pattern is going to be encoded within the toggle mode exclusively. Moreover, all hold latches have to be properly initialized. Consequently, a control signal First cycle produced at the end of the ring generator initialization phase reloads all latches with the current content of this part of the decompressor.

![Fig. 3 LP decompressor](image)

**IV. SIMULATION RESULTS**

![Fig. 4 LP decompressor](image)

**V. CONCLUSION**

As shown in the paper, the newly proposed low power PRPG is capable of acting as a fully functional test data decompressor with ability to precisely control scan shift-in switching activity through the process of encoding, while its low power test logic requires considerably smaller amount of silicon real estate than that of the existing low power compression schemes. The proposed hybrid solution allows one to efficiently combine test compression with logic BIST, where both techniques can work synergistically to deliver high quality test. It is therefore a very attractive low power test scheme that allows for trading-off test coverage, pattern counts and toggling rates.

**VI. REFERENCES**


